Threshold Voltage Performance Modelling for 3D FD SOI MOSFET with Back Gate Bias

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Abstract:
The threshold voltage of semiconductor devices changes because of SCE when a Fully Depleted SOI MOSFET is scaled in nanometer state. For controlling threshold voltage, vary the back gate bias and thickness of the oxide of back gate. In this work, mathematical modeling with three dimension of threshold voltage with SOI MOSFET is presented. The method, separation of variable is used to calculate the 3-Dimensional poisson's equation, analytically with suitable boundary conditions for Double Gate SOI MOSFET and applying a back gate voltage. When oxide thickneess of back gate is lesser than the critical thickness as per back gate voltage, threshold voltage will be less as SOI film thickness is reduced, because of capacitive coupling between back gate and SOI layer. Due to this fact, the fluctuations in threshold voltage because of the thickness variation in SOI film, are getting reduced by optimizing the thickness of back gate oxide by controlling the back gate voltage.

Keywords: FD Silicon on insulator technology, Three Dimensional analytical model, SCE, back gate voltage control.

Abbreviations: FD, fully depleted; SCE, short channel effect; DG, double gate; SOI, silicon on insulator.

1. INTRODUCTION

For performance of good device speed and better integration densities, scaling of the semiconductor devices has to be done. But due to scaling, there will be degradation in the characteristics of a MOSFET. Still, Bulk CMOS technology will stay for submicron gate ULSI systems. A new technology has taken up the place of BULK CMOS that is Double gate SOI MOSFETs. These DG SOI MOS fabricated with very thin silicon film layer will have excellent electrical performances because DG SOI MOSFETs will have excellent latch-up immunity, better control of SCE, boost isolation and decreased parasitic capacitances as compared with other technology [1].

To improve performance of semiconductor devices during scaling, there is a requirement of suppression of SCE so as to have better reliability of semiconductor devices[3,4].

When the channel length reduces to nanometer, controlling power of gate over the depletion region of channel of MOSFET reduces and give rise to charge sharing from source region and drain region of MOSFET[6-8]. Many reliability issues takes place because of SCE like change in threshold voltage with respect to channel length occurs and pinch off condition in channel. There are many ways to minimize the SCE like control of SCE by double gates, thinner gate oxide thickness and by applying back gate voltage.

In this paper, a new model is developed which is based on threshold voltage for FD DG SOI MOSFET by using separation of variable method for solving the three dimensional poisson's equation and calculate the effects of both front and back gates bias on the threshold voltage of DG SOI MOSFET. Drain voltage effect is also included in study.

2. MOSFET WITH SOI TECHNOLOGY

Technology from Bulk MOSFET switched to SOI MOSFET as there are various benefits of SOI technology like high device density, latch up elimination, very low leakage current, very high speed of operation, small power dissipation, easy device isolation structure [2] etc.

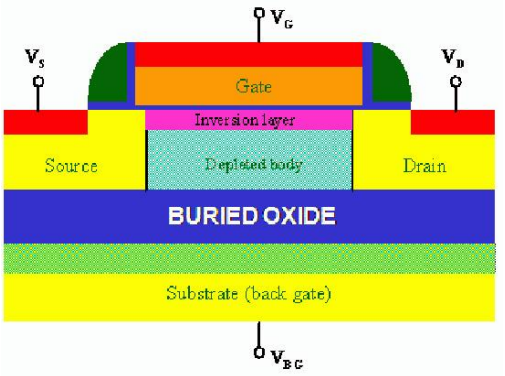

Fig 1: DG SOI MOSFET with back gate bias

Analyze the DG SOI MOSFET structure, the interface of front interface of silicon-silicon oxide is set at x=0 and the back interface of silicon-silicon oxide interface is set at x= t_{si}

To solve the expression of 3D Poisson's equation is:

$$\frac{\partial^2\Psi(x,y,z)}{\partial x^2}+\frac{\partial^2\Psi(x,y,z)}{\partial y^2}+\frac{\partial^2\Psi(x,y,z)}{\partial z^2}=-\frac{\rho(x,y,z)}{\varepsilon_{si}} \quad (1)$$

Here, $\Psi(x,y,z)$ is the potential in the SOI film at a particular point x,y,z and $\rho(x,y,z)$ is the 3-dimensional charge density in the SOI film is marked at a point x,y,z. Now, Separate equation (1) into 1-Dimension Poisson's equation**,** 2-Dimensional and 3-Dimensional Laplace equation, we get

$$\frac{\partial^2\Psi1(x)}{\partial x^2}=-\frac{\rho(x)}{\varepsilon_{si}} \quad \textbf{(2)}$$

$$\frac{\partial^2\Psi2(x,y)}{\partial x^2}+\frac{\partial^2\Psi2(x,y)}{\partial y^2}=0 \quad \textbf{(3)}$$

$$\frac{\partial^2\Psi3(x,y,z)}{\partial x^2}+\frac{\partial^2\Psi3(x,y,z)}{\partial y^2}+\frac{\partial^2\Psi3(x,y,z)}{\partial z^2}=0 \quad \textbf{(4)}$$

where,

$$\Psi(x,y,z)=\Psi1(x)+\Psi2(x,y)+\Psi3(x,y,z) \quad \textbf{(5)}$$

$\Psi_l(x) \rightarrow$

$$\Psi1(x)=\Psi_b+E_b(t_{si}-x)+\frac{qN_a}{2\varepsilon_{si}}(t_{si}-x)^2 \quad \textbf{(6)}$$

$\Psi_2(x,y) \rightarrow$

$$\Psi2(x,y)=\frac{1}{\sinh(\alpha_m L_{eff})}\left[V'_m\sinh(\alpha_m y+ Vm\sinh\alpha m(Leff-y\sinh(\alpha mx)+\varepsilon si\varepsilon ox toxf\alpha m\cos(\alpha mx)\right] \quad \textbf{(7)}$$

$\Psi_3(x,y,z) \rightarrow$

$$\Psi3(x,y,z)=\sum_{m=1}^{\infty}\sum_{p=1}^{\infty}\left[G_{mp}\cosh(\alpha_{mp}z)+H_{mp}\sinh(\alpha_{mp}z)\right]\frac{\sin(\alpha_m(y-L_{eff}))}{\cos(\alpha_m L_{eff})}\left[\sin(\alpha_p x)+\frac{\varepsilon_{si}}{\varepsilon_{ox}}t_{oxf}\alpha_p\cos(\alpha_p x)\right] \quad \textbf{(8)}$$

3. THRESHOLD VOLTAGE MODEL WITH BACK GATE VOLTAGE, V_{bg}, FOR SOI MOSFET

To enhance scalability of MOSFET technology, we can use the ultrathin (UT) body and buried oxide (BO) thickness to provide the better control of Short Channel effects. The control of threshold voltage can be done by the voltage of back gate as there is a strong coupling effect between back gate to front gate of the device [14-16] and the use of different concentration of channel doping is not needed to control of threshold voltage[17-19,21] and we can avoid the changes occur due to the fluctuations of random dopants.

Simulation tool with high accuracy is required to exploit the advantages of Fully Depleted SOI with ultrathin (UT) body and ultrathin (UT) box transistors[9-11]. The very important device parameter is the threshold voltage, which is used for the modeling of drain current compactly and low frequency noise.

The 2-D charge sharing concept has been proposed for analytical modeling of the threshold voltage for fully depleted-SOI MOSFET[12,13]. In this concept, there is a charge sharing between the gate region and source-drain regions, which leads to the underestimate threshold voltage roll off. The 2-D Poisson's equation get solved by the techniques three-zone Green's function for determining both (front and back) surface potential from which the expression of threshold voltage was derived [20]. These methods are suitable for the limit of the channel length down to 0.1μm.

Threshold voltage models for SOI MOSFET is developed using Poisson's equation at the interface of silicon body front gate and front gate, 2-dimension potential was derived in the silicon body [25]. For asymmetrical Fully Depleted-SOI MOSFET, an

analytical threshold voltage model has been suggested which depends on the lateral variations of the both surface potentials [26]. As per this , threshold voltage is a voltage on gate when surface potential becomes two times of Fermi potential from midgap. But for modern devices, this statement of threshold voltage is not suitable for silicon body (undoped) with short length of channel. Recently, a new model of threshold voltage [22-24,27] was developed for undoped symmetric DG MOSFET. In this model, the effect of interface roughness and voltage at back gate at the threshold voltage is included. In the same method, iteration method is using to determine the threshold voltage, which comprises parameters derived by solutions of other equations.

The expression for threshold voltage for silicon in insulator MOSFET with back gate voltage is expressed as

$$V_{fg} = V_{fbf} + \left(1 + \frac{C_s + \mathrm{C_{itf}}}{C_{fox}}\right)\Psi_f - \frac{C_s}{C_{fox}}\,\Psi_b - \frac{Q_{eff} - 2q\sum_{s=1}^{n} N_{As}t_s}{2C_{fox}} \quad \textbf{(9)}$$

and

$$V_{bg} = V_{fbb} + \left(1 + \frac{C_s + \mathrm{C_{itb}}}{C_{box}}\right)\Psi_b - \frac{C_s}{C_{box}}\,\Psi_f + \frac{Q_{eff}}{2C_{box}} - \mathrm{V_b} \quad \textbf{(10)}$$

Now substitute the value of $\Psi_f = 2\varphi_{sf}$, $\mathrm{V_b} = 0$ and $\Psi_b = \Psi_{bA}$ in above equation 10 to obtain the value of V_{bgsbA} which is equivalent to V_{bg} corresponding to Ψ_{bA}, with the condition that the front gate is in inversion state.

Likewise, substitute the value of $\Psi_f = 2\varphi_{sf}$, $\mathrm{V_b} = 2\varphi_{sb}$ and $\Psi_b = \Psi_{bI}$ in above equation 10 to obtain the value of V_{bgsbI} which is equivalent to V_{bg} corresponding to Ψ_{bI}, with the condition that the front gate is in inversion state. And from equation 11 , we get the value of φbf.

$$\varphi_{\mathrm{bf}} = \mathrm{V_t} \ln \frac{\mathrm{N_{A1}}}{\mathrm{n_i}} \quad \textbf{(11)}$$

The silicon on insulator substrate operates in three different modes[28-32]. For a corresponding value of back gate voltage, $\mathrm{V_{bg}}$, the value of Ψ_b depends upon the different modes in which the SOI substrate is operating. The procedure of calculating the value of Ψ_b for a corresponding value of back gate voltage,$\mathrm{V_{bg}}$ at three different modes of operation are given as:

Case I: when the SOI substrate in accumulation state, $V_{bg} \geq V_{bgsbA}$

In this accumulation state of operation, the voltage drop in substrate is 0, $\mathrm{V_b} = 0$. From above equation 10, we can obtain the value of Ψ_b at any value of back gate voltage, $\mathrm{V_{bg}}$ with $\mathrm{V_b}$= 0 and Ψ_f=2 φbf

Case II: when the SOI substrate in inversion state, $V_{bg} \leq V_{bgsbI}$

In this inversion state of operation, the voltage drop in substrate is $2\varphi_{sb}$, $\mathrm{V_b} = 2\varphi_{sb}$. From the equation 10, we can obtain the value of Ψ_b at any value of back gate voltage, $\mathrm{V_{bg}}$ with $\mathrm{V_b}$= $2\varphi_{sb}$ and Ψ_f=2 φbf.

Case III: when the SOI substrate in depletion state, $V_{bgsbA} > V_{bg} > V_{bgsbI}$

In this depletion state of operation, the voltage drop in substrate lies from 0 to $2\varphi_{sb}$, $0<\mathrm{V_b}<2\varphi_{sb}$. From the equations 10, we can obtain the value of Ψ_b at any value of back gate voltage, $\mathrm{V_{bg}}$ with Ψ_f=2 φbf. (3.84)

Now obtain the value of Ψ_b at a particular value of back gate voltage, V_{bg} by identifying SOI substrate mode in which it is operating and there is a particular procedure for different types of modes, which is going to be followed. After that, threshold voltage, Vt is obtained at a particular value of back gate voltage, V_{bg} by putting the value of Ψ_b in the equation given below:

$$V_t = V_{fbf} + \left(1 + \frac{C_s + \mathrm{C_{itf}}}{C_{fox}}\right)2\varphi\mathrm{bf} - \frac{C_s}{C_{fox}}\,\Psi_b - \frac{Q_{eff} - 2q\sum_{s=1}^{n} N_{As}t_s}{2C_{fox}} \quad \textbf{(12)}$$

4. RESULTS AND DISCUSSIONS

The threshold voltage [5,11] is defined as the gate voltage at which significant current starts to flow from the source to the drain. Experimental values used: t_{si}=15nm, t_{oxf}=2nm, t_{oxb}=30 nm, N_A=1×10^{17}/cm^3 at V_{ds}=1V, V_{bg}=-2V.

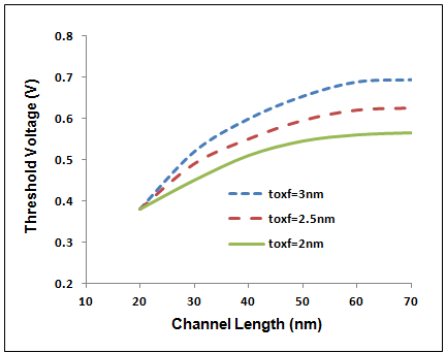

Fig 2: Variation in V_{th} with channel length for t_{oxf}

Fig 2 shows that slope shift downwards as the front gate oxide thickness reduces, ie Threshold voltage can be control with a combination of channel lenght and gate oxide thickness.

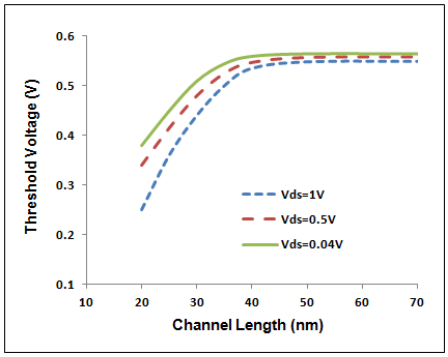

Fig 3: Variation in V_{th} wrt channel length for different V_{ds}.

Fig 3 shows that slope is shifting downwards for lower values of drain to source voltage, ie Threshold voltage can be control with a combination of channel lenght and drain to source voltage.

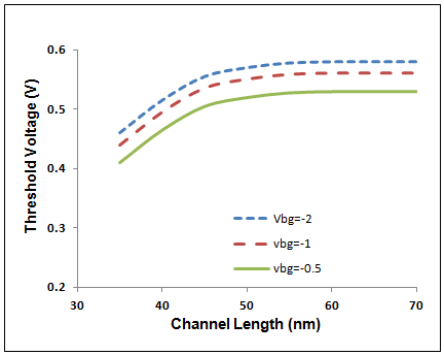

Fig 4: Variation in V_{th} wrt channel length for different V_{ds}.

Fig 4 shows that slope shifts downwards for lower values of back gate bias voltage**.**

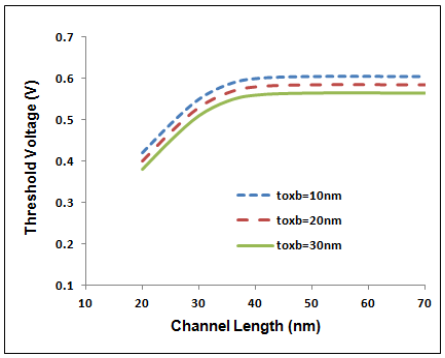

Fig 5: Variation in V_{th} wrt channel length for different t_{oxb}.

Fig 5 Shows that slope shifts downwards for higher values of back gate oxide thickness denotes control of threshold voltage.

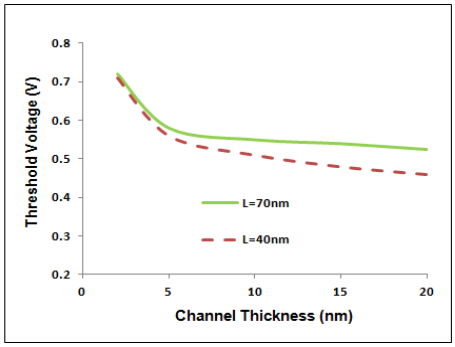

Fig 6: Change in V_{th} along channel thickness for channel length

Fig 6 Shows that slope shifts downwards, hence controlling of threshold voltage for lower values channel length.

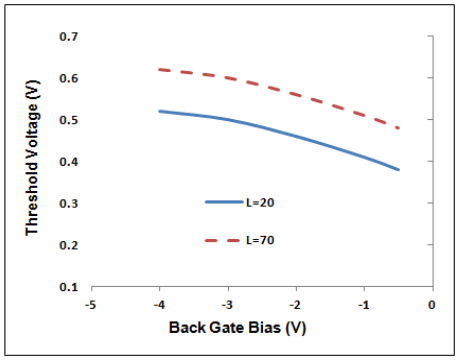

Fig 7: Change in V_{th} with V_{bg}.

Fig 7 shows that threshold voltage decreases with more bias voltage and Slope shift downward for lower values of channel length.

5. CONCLUSION

The effects of front and back gate control on the threshold voltage for FD SOI MOSFET has been presented using MATCAD 13. This result has been experimentally verified by using 3D ATLAS software that back gate voltage controls the performance of device and is used to suppress the effects of short channel effect and performance of device is improved. Threshold voltage behavior with Channel thickness shows better control with 70nm channel length, threshold voltage degrades as channel length reduces shown in Fig 6**.** Back gate bias controllability with threshold voltage is given in Fig 7, shows incremental changes with respect to bias voltage.

When oxide thicknesss of back gate is lesser than the critical thickness as per back gate voltage, threshold voltage will be less as SOI film thickness is reduced, because of capacitive coupling between back gate and SOI layer.

6. Future Scope

Work in this field can be explore further as only few work has been done so far, expected future work scope can be listed as below,

Multiple Gate Structure can be explore for achieving further performance improvement and have better reliability.

Here in this work Threshold voltage behavior is analyzed which can be extended to explore capacitance variation and impact of frequency, Hence switching performance can be analyzed.

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